REMARKS

Claims 1-11 are pending in the present application. Claims 1-8 stand rejected under 35 U.S.C. §102(b) as being anticipated by United States Patent No. 4,212,059 to Sato et al. ("the Sato reference"). It is respectfully submitted that Claims 1 - 11 are not anticipated by the Sato reference for at least the following reasons.

In response to Applicants' previous response to this rejection, the Examiner replied as follows:

> Applicants argue that the Sato reference does not teach, "executing an auxiliary program in the alternate memory." Applicants argue that Sato in fact teaches executing the auxiliary program in same memory as the normal processing routine. The examiner respectfully disagrees. The examiner believes that the actual execution of the program must take place in the processor, i.e. the processor retrieves the instructions of the program from the memory and then executes them. **The examiner therefore believes that the Sato reference teaches the processor taking the instructions for the "abnormal processing routine" from the alternate memory (the flexible disk unit of Sato), transferring these instructs to an area in the processor and executing them.** The examiner believes that this is equivalent in function to applicants' claimed invention. The examiner believes applicants' claimed invention switches to the claimed alternate memory, takes the program instructions from the alternate memory area and executing the instructions in the processor. The examiner therefore maintains the rejection of claim 1 using the previously provided reference to Sato. (Office Action, p. 5, l. 10 – p. 6, l. 2). (*emphasis added*).

Independent Claim 1 recites:

> A method for checking a functioning of a computer, the computer, **in a normal operating state, accessing a working memory using bus lines**, a content of the working memory being able to be influenced by a user, the method comprising the steps of:
>
> **diverting an access of the computer, by a switchover device, such that the access is directed to an alternate memory rather than to the working memory**; and
>
> executing an auxiliary program in the alternate memory when activated by the computer, the auxiliary program making available information concerning internal operating states of the computer. (*emphasis added*).

Thus, according to Claim 1, computer access to the working memory is **diverted** to an alternate memory, and **the auxiliary program is executed in the alternate**

memory; the auxiliary program is not executed in the working memory. It should be noted that Claim 1 does not require that the entire working memory be diverted. (See also Specification, p. 2, ll. 20-23). However, Claim 1 does recite that at least part of the working memory is diverted to an alternate memory. The Sato reference fails to disclose diverting access to any memory.

The Sato reference discloses the following: (1) the operation console is comprised of an operation processor, a flexible disk storage unit, a CRT display, and a keyboard (Sato, col. 3, ll. 24 – 26); (2) the operation processor comprises a microprocessor 300 and memories 301 to 303 (Sato, col. 3, ll. 26 – 27); (3) the flexible disk stores both the abnormal and normal processing routines (Sato, col. 9, ll. 53 – 58); (4) for execution, the abnormal processing routine is read out from the flexible disk onto the overlay area for execution (Sato, col. 9, ll. 44 – 49). Thus, both the normal and abnormal routines are stored on the flexible disk, and the execution of both routines occurs in processor memories 301-303.

As applied to Claim 1, memories 301 – 303 of Sato comprise the working memory for the processor, and, as asserted by the Examiner, the flexible disk is the alternate memory. Under this construction, the Sato reference does not disclose diverting access from the working memories 301-303, or any part thereof, to the alternate memory, and then executing an auxiliary program in the alternate memory. Indeed, the Examiner acknowledges that the processor executes both programs in the processor's working memory (memories 301-303).

Since the Sato reference fails to disclose diverting the computer away from the working memory and executing the abnormal processing routine in the alternate memory, the Sato reference does not disclose each and every feature of Claim 1. Thus, the Sato reference does not anticipate Claim 1 or its dependent Claims 2-8. It is therefore respectfully requested that this rejection be withdrawn.

Claims 9-11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the Sato reference in view of United States Patent No. 6,105,102 to Williams et. al. ("the Williams reference"). Claims 9-11 depend from Claim 1. As discussed above in reference to Claim 1, the Sato reference fails to disclose "diverting an access of the computer, by a switchover device, such that the access is directed to an alternate memory rather than to the working memory." The Williams reference similarly fails to teach or suggest this limitation. Since the Sato and Williams references fail to disclose each and every feature of Claim 1, the

Sato and Williams references do not render dependent Claims 9-11 obvious under 35 U.S.C. §103(a). It is therefore respectfully requested that this rejection be withdrawn.

CONCLUSION

In light of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully Submitted,

Dated: 7/11/07

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